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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,676	07/02/2003	Thomas C. Anthony	10014296-1	3426

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EXAMINER	
TRAN, LONG K	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,676	ANTHONY ET AL.	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 33* is/are pending in the application.

4a) Of the above claim(s) *18 - 28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 17 and 29 - 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/02/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group **I**, Claims **1 – 17** and **29 – 33** in the reply filed on October 15, 2004 is acknowledged.

Because Applicants did not distinctly and specially point out the supposed error in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Applicants have the right to file a divisional application covering the subject matter of non-elected claims.

Information Disclosure Statement

2. This office acknowledges of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on July 02, 2003.

The references cited on the PTO -1449 form have been considered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims **1 – 3** and **8 – 10** are rejected under 35 U.S.C. 102(e) as being anticipated by Childress et al. (US Patent Application Publication No. 2003/0231437).

5. Regarding claim **1**, Childress et al. disclose a memory wafer ([0018]) comprising:

a first surface of 9, 109 (figs. 1 & 2) having memory chips disposed thereon, the memory chip defining an exterior face 150 (fig. 2) of the memory wafer;

A second surface of 9, 109 (figs. 1 & 2) opposite the exterior face; and

A top magnetically permeable shield layer on top of surface 150 (not shown) ([0021]).

Regarding claim **2**, Childress et al. disclose the memory chips are separable from the memory wafer (fig. 1).

Regarding claim **3**, Childress et al. disclose the memory chips are MRAM ([0002]).

Regarding claims **8** and **9**, Childress et al. disclose the magnetically permeable layer is a permalloy (NiFe) and is a soft magnetic material.

6. Claims **13, 14** and **17** are rejected under 35 U.S.C. 102(e) as being anticipated by Rizzo et al. (US Patent Application Publication No. 2004/0000415).

7. Regarding claim **13**, Rizzo et al. disclose memory chip 15 (fig. 1) separated from a memory wafer ([0039]), the memory chip comprising:

At least one memory array 14 (fig. 1) positioned between an exterior chip face and a second chip surface opposite the exterior chip face; and

A magnetically permeable shield layers 30 (fig. 7) and 26 (fig. 7; ([0032]) extending over the exterior chip surface and the second chip surface 21 (fig. 7).

Regarding claim **14**, Rizzo et al. disclose integrated circuit 15 (fig. 1; ([0025]) including contact pads capable of transmitting signals to and from circuit 15 ([0025]).

Regarding claim **17**, Rizzo et al. disclose the magnetically permeable shield layer is isotropic ([0053]).

Regarding claim **31**, Rizzo et al. disclose a shielded integrated circuit being compatible with portable electronic system ([0056]) comprising an electronic device (note: Rizzo et al. silent on an electronic device and a memory chip electrically connected to the electronic device. However it's understood by one of ordinary skill in the art at the time the invention was made, a portable electronic device using memory chip has to have a electronic device and electrically connected to the memory chip to make the system working); and memory chip 15 (fig. 1) separated from a memory wafer ([0039]), the memory chip comprising:

At least one memory array 14 (fig. 1) positioned between an exterior chip face and a second chip surface opposite the exterior chip face; and

A magnetically permeable shield layers 30 (fig. 7) and 26 (fig. 7; ([0032]) extending over the exterior chip surface and the second chip surface 21 (fig. 7).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims **4, 5, 6, 7,10,11** and **12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Childress et al. (US Patent Application Publication No.

2003/0231437) in view of Rizzo et al. (US Patent Application Publication No. 2004/0000415).

10. Regarding claim **4**, Childress et al. disclose the claimed invention of claim 1 except for the memory chips include multiple memory arrays having multiple memory cells.

It is conventional and also shown by Rizzo et al. that MRAM including an array of magnetic memories ([0025]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to understand that Childress's device would comprise multiple memory arrays having multiple memory cells since it was known in the art that MRAM including cells in array.

Regarding claim **5**, Childress et al. disclose the memory cells are magnetic random access cells ([0002], [0018]).

Regarding claims **6** and **7**, Rizzo et al. disclose integrated circuit 15 (fig. 1; ([0025]) including contact pads capable of transmitting signals to and from circuit 15 ([0025]).

Regarding claim **10**, Rizzo et al. disclose the magnetically permeable shield layer has a permeability of 1,000 – 10,000 ([0053]).

Regarding claim **11**, Rizzo et al. disclose the magnetically permeable shield layer has a coercivity of less than 10 Oersteds ([0043]).

Regarding claim **12**, Rizzo et al. disclose the magnetically permeable shield layer is isotropic ([0053]).

11. Claims **15** and **16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Rizzo et al. (US Patent Application Publication No. 2004/0000415) in view of Tuttle et al. (US Patent Application Publication No. 2003/01322494).

Regarding claim **15**, Rizzo et al. disclose the claimed invention of claim 13 except for the memory chip is contained in an integrated circuit package.

Tuttle et al. show a magnetic integrated circuit 12 (fig. 1) with housing 10 (fig. 1) forming an integrated circuit package.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide package or housing for Rizzo's integrated circuit as taught by Tuttle at al. in order to protect the integrated circuit from damaging.

Regarding claim **16**, Tuttle et al. disclose the integrated circuit package including support for the memory chip, electrical wires connected to a leading away from the memory chip, and an insulating package encapsulating at least the memory chip (fig. 1; ([0026], [0027] and [0028]).

12. Claims **29** and **30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Childress et al. (US Patent Application Publication No. 2003/0231437) in view of Tuttle et al. (US Patent Application Publication No. 2003/01322494).

Regarding claim **29**, Childress et al. disclose a memory wafer ([0018]) comprising:

a first surface of 9, 109 (figs. 1 & 2) having memory chips disposed thereon, the memory chip defining an exterior face 150 (fig. 2) of the memory wafer;

a second surface of 9, 109 (figs. 1 & 2) opposite the exterior face; and

a top magnetically permeable shield layer on top of surface 150 (not shown) ([0021]).

Childress et al. do not explicitly show means for protecting the memory cells from stray magnetic fields.

However, Tuttle et al. show the undesirable external magnetic field can also call stray fields ([0019]). The magnetically permeable foils 26 and 28 (fig. 1) are attached to top and bottom outer surfaces of the chip used as shields from stray fields ([0028]). The magnetically permeable layers of Childress device are identical to Tuttle shields. Therefore they can be used as means for protecting from external field or stray fields.

Regarding claim **30**, Childress et al. disclose the magnetically permeable layer is a permalloy (NiFe) and is a soft magnetic material.

13. Claims **31** and **32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Childress et al. (US Patent Application Publication No. 2003/0231437) in view of Tuttle et al. (US Patent Application Publication No. 2003/01322494) and further in view of Rizzo et al. (US Patent Application Publication No. 2004/0000415).

14. Regarding claim **31**, Childress et al. and Tuttle et al. disclose the claimed invention of claims 29 and 30 except for the magnetically permeable shield layer has permeability of greater than 100.

Rizzo et al. show a shielding material can have a permeability1,000 – 10,000 depending on the particle size ([0051] and [0053]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the magnetically permeable shield layer of Childress and Tuttle with a layer having a permeability of greater than 100 as taught by in order to get superparamagnetic behavior for very effective magnetic field shielding.

Regarding claim **32**, Rizzo et al. disclose the magnetically permeable shield layer has a coercivity of less than 10 Oersteds ([0043]).

15. Claim **33** are rejected under 35 U.S.C. 103(a) as being unpatentable over Rizzo et al. (US Patent Application Publication No. 2004/0000415).

16. Regarding claim **33**, Rizzo et al. disclose a shielded integrated circuit being compatible with portable electronic system ([0056]) comprising memory chip 15 (fig. 12) connected to other device via contact pads 54, leads 56 and wire bonds 60 (fig. 12); wherein the memory chip comprising:

At least one memory array 14 (fig. 1) positioned between an exterior chip face and a second chip surface opposite the exterior chip face; and

A magnetically permeable shield layers 30 (fig. 7) and 26 (fig. 7; ([0032]) extending over the exterior chip surface and the second chip surface 21 (fig. 7).

Rizzo et al. do not explicitly show an electronic device and a memory chip electrically connected to the electronic device.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that a portable electronic device using memory chip has to have an electronic device that electrically connected to the memory chip to make the system working. Therefore, Rizzo's portable electronic system comprises an electronic device and a memory chip electrically connected to the electronic device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Tran

December 21, 2004

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